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Title:

REPAIR FUSE BOX OF SEMICONDUCTOR DEVICE

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REPAIR FUSE BOX OF SEMICONDUCTOR DEVICE

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a repair fuse box of a semiconductor device and, more specifically, to a repair fuse box having a structure in which a signal line can be drawn out from a repair fuse box without detour.

2. Discussion of Related Art

[0002] Recently, high-speed and highly integrated semiconductor devices have been developed with development of miniaturization technologies. In particular, high integration and high yield of semiconductor memory devices have been required, and in order to cope with the requirements, a redundancy technology, which improves a yield by providing redundancy circuits and repairing defective cells using the redundancy circuit, is essential.

[0003] In memory devices such as SRAM, DRAM, EPROM, and so on, redundancy circuits are provided in the semiconductor devices to prevent decrease of yields of the semiconductor devices due to process defects. The functions of the semiconductor devices are not damaged in spite of partial defects, by repairing defective cells using the provided redundancy circuits. That is, by providing a spare memory array as a redundancy circuit and

switching a main memory array into the spare memory array when the main memory array is defective, decrease of production yield can be regulated.

[0004] The redundancy circuit comprises a repair address generating circuit. A conventional repair address generating circuit has a structure shown in Fig. 1, and its operation will be explained briefly as follows.

[0005] A fuse set A comprises a plurality of fuses R0 to R15.

[0006] When an enable signal Enable is in a high state, a PMOS transistor P1 is turned off, and thus its output Out holds a low state.

[0007] When the enable signal Enable is in a low state, the output Out is changed in accordance with fuse control signals Fuse <0> to Fuse <15> and cutting states of the fuses R0 to R15.

[0008] For example, when the fuse control signal Fuse <0> is in a high state and the first fuse R0 is not cut, the NMOS transistor Q0 is turned on. Then, an output of a latch 10 is in a high state, and thus an output of the inverter I1 turns to a low state, so that the output Out turns to a low state. However, when the fuse R0 is cut, the output Out turns to a low state even if the fuse control signal Fuse <0> turns to a high state.

[0009] When forming the fuses in a fuse box shape to form the repair address generating circuit, metal signal lines cannot pass over the fuse box. Therefore, the metal signal line should detour around the fuse box for signal routing, and this make a chip size larger.

SUMMARY OF THE INVENTION

[0010] In order to solve the above problems, the present invention is directed to a repair fuse box of a semiconductor device.

[0011] According to an aspect of the present invention, there is provided a repair fuse box of a semiconductor device comprising: a plurality of fuse boxes arranged in a longitudinal direction, each fuse box comprising a plurality of fuses arranged in a transverse direction; signal connecting fuses arranged in each side portion of outermost fuses of the fuses which are selected from the fuses arranged in one or more fuse boxes of the plurality of fuse boxes to construct a unit fuse set and of which one side ends are connected mutually, the signal connecting fuses being connected to the outermost fuses; and metal lines for connecting the signal connecting fuses to the fuses selected to construct a unit fuse box in an upper or lower fuse box.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0013] Fig. 1 is a circuit diagram of a conventional repair address generating circuit;

[0014] Fig. 2 is a circuit diagram of a repair address generating circuit according to the present invention; and

[0015] Fig. 3 is a layout diagram of a repair fuse box circuit according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] Now, the present invention will be described in detail with reference to the accompanying drawings.

[0017] Fig. 2 is a circuit diagram of a repair address generating circuit according to the present invention.

[0018] The repair address generating circuit according to the present invention further comprises signal connecting fuses R16 and R17. The signal connecting fuses R16 and R17 can be made of any kind of materials as long as it is a conductive material. The operation of the circuit is not different from the operation of the conventional circuit. The operation will be described.

[0019] A fuse set B comprises a plurality of fuses R0 to R15 and signal connecting fuses R16 and R17.

[0020] When an enable signal Enable is in a high state, a PMOS transistor P1 is turned off, and thus an output Out of the circuit always holds a low state.

[0021] When the enable signal Enable is in a low state, the output Out of the circuit is changed in accordance with the fuse control signals Fuse <0> to Fuse <15> and the cutting states of the fuses R0 to R15.

[0022] For example, when the fuse control signal Fuse <0> is in a high state and the first fuse R0 is not cut, the NMOS transistor Q0 is turned on. Then, an output of a latch 10 is in a high state, and thus an output of the inverter I1 is in a low state, so that the output Out of the circuit turns to a low state. However, when the fuse R0 is cut, the output Out of the circuit turns to a low state even if the fuse control signal fuse <0> is in a high state.

[0023] Fig. 3 is a layout diagram of the repair fuse box according to the present invention for explaining how the fuses of the fuse set B of Fig. 2 are embodied in a substrate.

[0024] Fuse boxes 20, 30 and 40 are shown in Fig. 3. The configuration of the fuse set B for constructing the circuit of Fig. 2 will be explained as follows.

[0025] The fuses R0 to R4 are arranged in the fuse box 20, and a signal connecting fuse R16 is arranged to the left side of the fuse R4. Upper end portions of the fuses R0 to R4 and the signal connecting fuse R16 are connected together through a metal, and so on.

[0026] In the same manner, the fuses R5 to R9 are arranged in the fuse box 30, and a signal connecting fuse R17 is arranged to the left side of the fuse R9. Lower end portions of the fuses R5 to R9 and the signal connecting fuse R17 are connected together through a metal, and so on.

[0027] The signal connecting fuses R16 and R17 are connected together through a metal line M by using a contact process, and so on.

[0028] The fuses R10 to R15 are arranged in the fuse box 40. Upper end portions of the fuses R10 to R15 are not only connected together through a metal, and so on, but also connected to the fuse box 30.

[0029] As a result, one side nodes of the fuses R0 to R15 shown in Fig. 2 are all connected each other through the signal connecting fuses R16 and R17.

[0030] It should be noted that opened terminals of the fuses are connected to transistors.

[0031] Since the signal connecting fuses R16 and R17 are used for signal connection, they are not the cutting targets.

[0032] According to the present invention as described above, it is possible to connect the fuses without detour of the metal lines by using the fuse boxes.

[0033] As a result, since the signal routing can be implemented by using the fuses, it is possible to considerably reduce a chip size.

[0034] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood by the ordinary skilled in the art that changes and modifications of the present invention may be made without departing from the spirit and scope of the present invention and appended claims.